**In the Claims:**

1-14.      (canceled)

15.    (new)  A  process  for  testing  a  circuit  having  both  a
vendor  embedded  circuit  core  and  appended  user  circuitry,
using  ATPG  software  to  generate  test  vectors  therefore,
comprising:

 A.    generating  a  partial  netlist  of  the  entire  vendor
circuit;

 B.    define  at  least  one  pseudo-pin  input  for  at  least
some  of  the  circuitry  in  the  partial  netlist;

 C.    identify  an  output  node  of  the  vendor  circuit  to
which  the  user  circuitry  will  be  connected;

 D.    generate  an  abbreviated  core  netlist  of  the
vendor  circuit  that  includes  the  pseudo-pin  input  and  the
output  node  to  produce  outputs  at  the  output  node  in
response  to  an  input.


16.    (new)  The  process  of  claim  15  in  which  the  pseudo-pins
are  substituted  into  the  core  netlist  for  at  least  some  of
the  circuitry.